PIXELPLUS CO., LTD.

1/3 inch NTSC/PAL CMOS Image Sensor with D1 class Pixel array and Wide dynamic range

Xkhan™

WDR Image Sensor

Single chip SoC WDR Technology

PX2089K

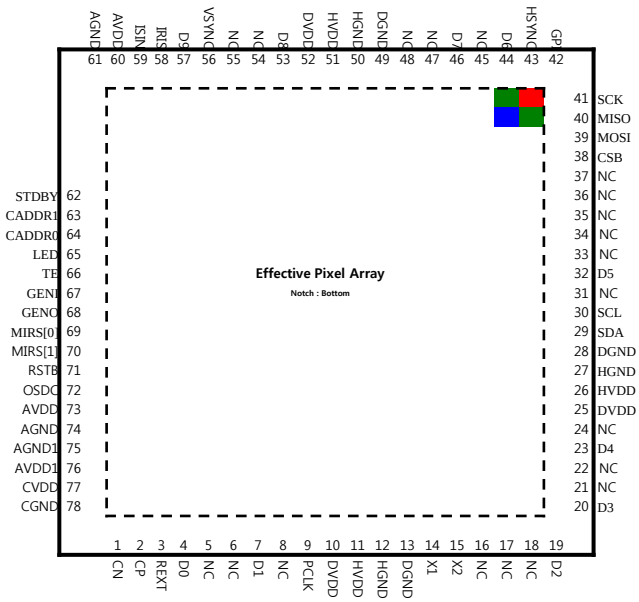
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1/3 inch NTSC/PAL CMOS Image Sensor with D1 class Pixel array and Wide dynamic range

Features

- ▷ 756 x 504 effective pixel array with RGB Bayer color filters and micro-lens
- ▷ Power supply
  AVDD : 3.3V, HVDD : 3.3V, CVDD : 3.3V
- ▷ Output formats
  - ◆ Composite Output mode
    - CVBS (NTSC/PAL)
  - ◆ Digital Output mode
    - max. D1 (720x480) YCbCr422/RGB565/ RGB444 (progressive, 60 fps @ 54Mhz)
    - max. D1 (720x480) Bayer (progressive, 60 fps @ 27Mhz)
  - ◆ Analog/Digital Output mode
    - ITU-R. BT656 (720x240/288) (interlaced, 60 fields @ 27Mhz)
    - CVBS (30 fps @ 27Mhz)
- ▷ Image processing on chip
  Lens shading, Gamma/Defect/Color correction, Low pass filter, Color interpolation, Saturation, Edge enhancement, Brightness, Contrast, Special effects, Auto black level, Auto white balance, Auto exposure control and Back light compensation
- ▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus
- ▷ Free scaling (up & down)
- ▷ High Image Quality and Ultra low light performance
- ▷ I2C master include
- ▷ Motion detection support
- ▷ Alarm mode, Privacy mode support
- ▷ Artificial Intelligence power save mode
- ▷ Chip Address Selection PADs
- ▷ Horizontal / Vertical mirroring
- ▷ Image cropping & Digital Zoom
- ▷ 50Hz, 60Hz flicker automatic cancellation
- ▷ Software Reset
- ▷ External Sync (Gen. Lock) support
- ▷ Off-chip, On-chip Smart IR-LED control
- ▷ On-chip IRIS controller
- ▷ WDR (Wide Dynamic Range) function
- ▷ Crystal input support
- ▷ On chip regulator for DVDD
- ▷ CSP/CLCC/PLCC Package type supports



[Fig. 1] PIN Description

Effective Pixel Array	756(H) x 504(V)
Pixel Size	6.35 um x 7.4 um
Effective Image Area	4.8 mm x 3.73 mm (Diagonal 6.08 mm)
Optical Format	1/3 inch, RGB Bayer filter
Max. Clock frequency	54 MHz
Max. Frame Rate	60 fps @ 720x480, YCbCr, 54Mhz 60 fps @ 720x480, Bayer, 27Mhz 60 field @ 720x240(288), YCbCr, 27Mhz 30 fps @ CVBS, 27Mhz
Dark Signal	40.2 [mV/sec] @ 60°C
Sensitivity	11.9 [V/Lux.sec]
Power Supply	Analog : 3.3V HVDD : 3.3V CVDD : 3.3V
Power Consumption	452.2 [mW] @ Dynamic
	726.0 [uW] @ Standby
Operating Temp. (Fully Functional Temp.)	- 30 ~ 80 [°C]
SNR	47.9 [dB]

[Table 1] Typical Parameters

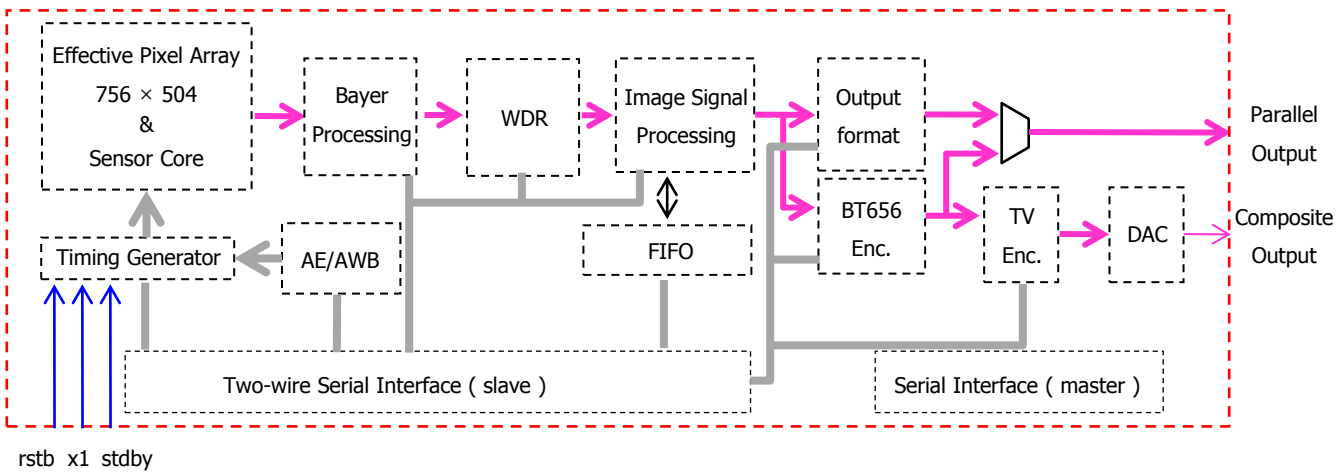
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▶ Signal Environment

PX2089K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended , it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PX2089K has 756 x 504 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 2] Block Diagram